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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/993,104 12/18/97 ROSENBERG

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EXAMINER

LM02/1228

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ART UNIT

PAPER NUMBER

2774

DATE MAILED:

12/28/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
08/993,104

Applicant(s)
SCOTT ROSENBERG ET AL.

Examiner
FRANCIS NGUYEN

Group Art Unit
2774



☒ Responsive to communication(s) filed on Nov 8, 1999

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire THREE month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-14 and 16-25 is/are pending in the application

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-14 and 16-25 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on Nov 8, 1999 is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 512

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2774

DETAILED ACTION

Response to Amendment

1. The amendment filed on 11/08/99 is entered. The proposed drawing correction filed on 11/08/99 is entered and approved by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-14,16-20, 22, 24-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. **Claim 1** recites the limitation “ first circuit configuration to substantially simultaneously and asynchronously drive respective positive and negative voltage signals ”(page 10, lines 2-3); the terms “substantially simultaneously and asynchronously ” and “ substantially predetermined rate ”(page 10, line 6) render the claim vague and indefinite. According to “Merriam-Webster’s Collegiate Dictionary”, simultaneous means **existing or occurring at the same time** (page 1094) and asynchronous means **not happening, existing or arising at precisely the same time** (pages 72 and 1196). The term substantially implies a certain tolerance allowed as related to the timing of driving voltage. **Putting those three terms together in the claim definitely causes the claim indefinite**

Art Unit: 2774

because it does not point out the subject matter which applicants regards as the invention ;
how would a timing diagram be drawn to illustrate those three combined concepts. The examiner reviewed the disclosure and found that the exact same terms were used(page 8, lines 15-18) without clear cut precise language; therefore the claim is vague and indefinite. As to limitation “substantially determined rate”, the disclosure provided unprecise language “substantially predetermined frequency”(page 67, line 25); **therefore, the Court case cited by Applicants does not apply here.**

5. **Claim 9** recites the limitation “ first circuit configuration to substantially simultaneously and asynchronously drive respective positive and negative voltage signals ” (page 10, lines 4-5) ; the terms “ substantially simultaneously and asynchronously ” and “ substantially predetermined rate ”(page 10, line 8) render the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).

6. **Claim 14** recites the limitation “ applying respective voltage signals to respective voltage signal storage elements substantially simultaneously and asynchronously, sampling the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate” (page 11, lines 2-5) ; the terms “substantially simultaneously and asynchronously” and “substantially predetermined rate” render the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).

Art Unit: 2774

8. **Claim 18** recites the limitation “ first circuit to substantially simultaneously and asynchronously drive respective positive and negative voltage signals ” (page 11, lines 2-3) ; the term “substantially simultaneously and asynchronously ” renders the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).
9. **Claim 20** recites the limitation “ second circuit is adapted to sample the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate ” (page 11, lines 2-3) ; the term “substantially predetermined rate” renders the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).
10. **Claim 22** recites the limitation “ applying respective voltage signals to respective voltage signal elements substantially simultaneously and asynchronously, and sampling the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate ” (page 12, lines 2-5) ; the terms “substantially simultaneously and asynchronously” and “substantially predetermined rate” render the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).
11. **Claim 24** recites the limitation “ first circuit configuration to substantially simultaneously and asynchronously drive respective positive and negative voltage signals ..., and a second circuit configuration to sample the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate ” (page 11, lines 4-8) ; the term “substantially simultaneously and asynchronously” and “substantially predetermined rate” render the claim vague and indefinite. The ground of rejection is maintained (see paragraph 4).

Art Unit: 2774

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 1 through 14, 16 through 25 are rejected under 35 U.S.C. 103(a) as being obvious over Takahara et al. (U.S. Patent 5,436,635) in view of Shields (U.S. Patent 4,870,396).

14. As to **claims 1, 9, 14, 18, 22, 24**, Takahara et al. discloses a circuit and associated method for modulating voltage signals comprising a first circuit configuration (**phase division circuit 42, source drive IC 11/12, figure 2**) to drive positive and negative voltage signals (V(P) and V(M), figure 3), and a second circuit configuration (**TFT as switching elements** for writing signal to pixel electrodes, column 6, lines 63-64, column 19, lines 36-38), changeover circuits 121/122 in figure 11, column 19, lines 55-65, column 20, lines 52-63) to alternatively sample the respective voltage signals at a substantially predetermined rate. However, Takahara et al. fails to expressly teach voltage signal storage elements. **Shields teaches voltage signal storage elements (storage capacitors 24, figure 4, column 2, lines 58-63) . It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus of Takahara et al., then add a voltage signal storage element to each pixel cell , as taught by Shields, to obtain the**

Art Unit: 2774

combined apparatus Takahara et al.-Shields because it would provide a sample and hold circuit, as taught by Shields(column 2, lines 58-60), and facilitate storage of video signal.

The terms simultaneously and asynchronously being used together cause indefiniteness, and contradiction; that is why the examiner chose not to use these terms together.

15. As to **claims 2, 3, 4, 5, 10, 11, 12, 13, 16 and 25**, Takahara et al.-Shields further teaches liquid crystal cell (see Shields, **liquid crystal cell LC in figure 4**), **circuitry to address said liquid crystal cell** (see Shields, **transistor 22**, figure 4), additional drive signals(see Takahara et al., transistors Tm11/Tm12/... in figure 1). One skilled in the art would know how to sample at a substantially predetermined rate as related to a particular liquid crystal material.

16. As to **claims 6, 7, 8 and 17**, Takahara et al.-Shields further teaches a plurality of transistors (see Shields, transistors 22 and 62 in figure 4) coupled to electrically isolate said voltage signal storage elements from said liquid crystal cell, and embodiment on an integrated circuit chip(see Takahara et al., column 13, lines 23-35).

17. As to **claims 19, 20, 21 and 23**, Takahara et al.-Shields teaches voltage signals comprising respective positive and negative voltage signals (see Takahara et al. , source drive IC (P) and source drive IC (M), figure 1), voltage sampling at a substantially predetermined rate (Shields, synchronous line-at-a-time loading, column 3, lines 12-19), voltage sampling so as to substantially maintain a substantially DC bias (Shields, AC activated displays , column 1, lines 36-39, applied RMS voltage across liquid crystal LC column 4, lines 10-11) . It would be obvious to a person of ordinary skill in

Art Unit: 2774

the art to arrange two respective voltage signal storage elements to accommodate respective positive and negative voltage signals because it would enable efficient storage of both voltage signals.

Response to Arguments

18. Applicant's arguments filed on 11/08/99 have been fully considered but they are not persuasive.

As to claims 1-20, 22, 24-25, Applicant's argument that these are definite. The examiner agrees with the cited Court case and M.P.E.P. section 2173.05(b). However, the examiner maintains the 35 U.S.C. 112 rejection because a review of the specification as related to limitations "substantially simultaneously and asynchronously", "substantially predetermined rate" indicates unprecise language (see details in paragraph 4). Therefore, the cited Court case does not apply here.

As to Applicant's argument on improper rejection, the examiner disagrees because the terms simultaneously and asynchronously putting together do not make sense (timing concept indefiniteness and contradiction). If the timing of driving voltage is crucial in the invention, how would that combined simultaneously-asynchronously feature be illustrated in a timing diagram? The examiner provided the explanation of obviousness in bold words in the rejections above. Again, note that Takahara et al. teaches a phase division circuit 42, source drive IC 11/12, as shown in figure 2 (this corresponds to the claimed circuit configuration for substantially simultaneously drive respectively positive and negative voltage signals), TFT and changeover circuits 121/122 (figure 11, column 19, lines 55-65, column 20, lines 52-63) which corresponds to the claimed second circuit configuration

Art Unit: 2774

to alternatively sample respective voltage signals. Shields is cited to teach the claimed voltage signal storage elements(capacitors 24, figure 4, column 2, lines 58-63). These limitations correspond to the independent claims 1, 9, 18 and 24. As to claims 14 and 22, note these same citations; note that Takahara et al.-Shield teaches AC activated display (Shields, column 1, lines 36-39), RMS voltage(Shields, column 4, lines 10-11) which implies a determined frequency.

It is suggested that the claims are specifically directed to structural means as shown in the drawin to illustrate the combined simultaneously-asynchronously feature.

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Francis Nguyen whose telephone number is (703) 308-8858. The examiner can normally be reached on weekdays from 8:00 AM to 4:30 PM.

Art Unit: 2774

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for this Group is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



Francis Nguyen

December 21st, 1999



RICHARD A. HJERPE
SUPERVISORY PATENT EXAMINER
GROUP 2700